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High-Bandwidth Memory Interface (SpringerBriefs in Electrical and Computer Engineering) 2014th Edition, Kindle Edition. by Chulwoo Kim (Author), Hyun-Woo Lee (Author), Junyoung Song (Author) & 0 more. Format: Kindle Edition. 5.0 out of 5 stars 1 rating. Part of: SpringerBriefs in Electrical and Computer Engineering (203 Books)

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Trends for further bandwidth enhancement are also covered. • Enables readers with minimal background in memory design to understand the basics of high-bandwidth memory interface design; • Presents state-of-the-art techniques for memory interface design; • Covers memory interface design at both the circuit level and system architecture level.

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High Bandwidth Memory is a high-speed computer memory interface for 3D-stacked SDRAM from Samsung, AMD and SK Hynix. It is used in conjunction with high-performance graphics accelerators, network devices and in some supercomputers. The first HBM memory chip was produced by SK Hynix in 2013, and the first devices to use HBM were the AMD Fiji GPUs in 2015. High Bandwidth Memory has been adopted by JEDEC as an industry standard in October 2013. The second generation, HBM2, was accepted by JEDEC in

[High Bandwidth Memory - Wikipedia](#)

High-Bandwidth Memory Interface. por Junyoung Song,Chulwoo Kim,Hyun-Woo Lee. SpringerBriefs in Electrical and Computer Engineering ¡Gracias por compartir! Has enviado la siguiente calificación y reseña. Lo publicaremos en nuestro sitio después de haberla revisado.

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J. Song et al., " An adaptive-bandwidth PLL for avoiding noise interference and DFE-less fast precharge sampling for over 10 Gb/s/pin graphics DRAM interface, " in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 2013, pp. 312–313. Google Scholar

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Bandwidth - Der Testsieger . Herzlich Willkommen auf unserer Webpräsenz. Die Betreiber dieses Portals haben es uns zur obersten Aufgabe gemacht, Varianten verschiedenster Art unter die Lupe zu nehmen, damit Sie als Kunde schnell den Bandwidth sich aneignen können, den Sie haben wollen.

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High-Bandwidth Memory Interface Design Chulwoo Kim ckim@korea.ac.kr Dept. of Electrical Engineering Korea University, Seoul, Korea February 17, 2013 Chulwoo Kim 1 of 86 . Outline Introduction Clock Generation and Distribution Transceiver Design TSV Interface for DRAM Summary

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